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Minimum Voltage for Threshold Switching in Nanoscale Phase-Change Memory

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ABSTRACT

The size scaling of the threshold voltage required for the amorphous-to-crystalline transition in phase-change memory (PCM) is investigated using planar devices incorporating individual GeTe and Sb_2Te_3 nanowires. We show that the scaling law governing threshold switching changes from constant field to constant voltage scaling as the amorphous domain length falls below 10 nm. This crossover is a consequence of the energetic requirement for carrier multiplication through inelastic scattering processes and indicates that the size of PCM bits can be miniaturized to the true nanometer scale.

The operation of PCM relies on electrically driving chalcogenide compounds between a conductive crystalline (ON) state and a highly resistive amorphous (OFF) state.[1−7] The ON-to-OFF RESET switching is typically achieved by applying a high voltage pulse with a short duration, which causes the memory cell to melt and rapidly quench into a glassy structure. The reverse SET switching is accomplished using a smaller voltage pulse with a longer duration and occurs through a two-step process:[8] during the first step, known as threshold switching,[9−11] an electric field induces carrier multiplication through inelastic scattering, causing the resistance of the amorphous phase to decrease. In turn, this drop in resistance allows appreciable current to flow and enables memory switching, in which the amorphous phase reaches a material-specific glass transition temperature (T_g) and recrystallizes. The promise of PCM has been demonstrated by researchers in both industry and academia:[1−7] PCM chips with an ultrathin film thickness (3 nm) and sub-50 nm cell size have been realized in industrial prototypes,[7] and programming times of less than 50 ns have been realized by choosing a phase-change material with a fast crystallization rate.[4]

Nevertheless, whether the size of the PCM bits can be pushed into the sub-10 nm scale remains unknown. On the basis of thermodynamic considerations, the minimum bit size is estimated to be as small as 2 nm.[12] However, previous studies[4,9,10,13] have also shown that the voltage required for threshold switching (V_{th}) decreases linearly with film thickness, leading to a material-specific critical electrical field (E_{th}) for SET operation ($E_{th} = 30-40$ and 14 V/μm for $Ge_2Sb_2Te_5$ and Sb_2Te_3, respectively).[4] Were this constant field scaling to continue to the nanometer scale, it would pose a serious problem for the stability of nanoscale PCM bits: assuming a typical value of E_{th} of ∼20 V/μm, V_{th} would fall below ∼0.1 V for PCM cells smaller than ∼5 nm. Such a small V_{th} not only reduces the readout window but also makes the data bits vulnerable to voltage fluctuations, leading to unintended data loss.

In this study, we investigate how V_{th} changes as the PCM bit size reaches the nanometer scale by employing planar PCM test beds that incorporate individual nanowires (NWs) of prototype phase-change materials, GeTe and Sb_2Te_3.[14−19] Compared to the vertical device architecture commonly employed in integrated memory devices,[3,8,20] planar devices[4,7,14−19] offer important advantages for fundamental studies. First, four-probe geometry can be easily realized in NW devices, enabling the disentanglement of metal-NW contact issues from the properties of the NW. Moreover, planar geometry is amenable to scanned probe techniques,[21,22] and thus the formation of amorphous and crystalline domains within a NW can be directly observed. These advantages are critical for discerning the domain structure and size scaling of V_{th} in nanoscale PCM devices. Although the initial NWs have higher crystallinity than the phase change materials in the PCM devices fabricated by top-down techniques, the recrystallized NWs are polycrystalline and the conclusion based on the NWs also applies to the top-down devices.

Crystalline GeTe and Sb_2Te_3 NWs used in this study were prepared using a vapor−liquid−solid method, as reported

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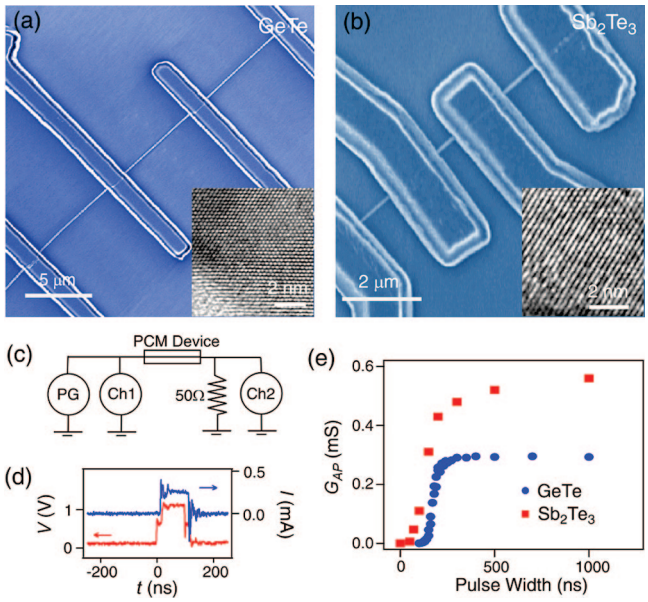

Figure 1. (a,b) SEM images of PCM devices incorporating individual GeTe and Sb_2Te_3 NWs, respectively. (Insets) High-resolution transmission electron microscope (TEM) images of respective NWs. (c) Schematic of the measurement circuit for temporal response (PG, pulse generator; Ch1, Ch2, channel 1 and 2 of the oscilloscope, respectively). (d) Voltage (V) and current (I) responses of a GeTe device to a SET pulse. (e) Low-bias conductance (G_{AP}) of amorphized GeTe and Sb_2Te_3 devices after SET pulses with different widths.

previously.[14−19] The PCM devices incorporating individual GeTe or Sb_2Te_3 NWs were made by standard electron beam lithography (see Supporting Information). Ohmic contacts to NWs were made by sputtering Cr/Au as metal electrodes. Figure 1a,b shows scanning electron microscope (SEM) images of representative GeTe and Sb_2Te_3 NW devices. The conductance response of GeTe and Sb_2Te_3 NWs to the back-gate voltage (applied to a degenerately doped silicon substrate) indicates that crystalline GeTe and Sb_2Te_3 NWs are p-type, with the carrier concentration (n) and the mobility (μ) for GeTe (Sb_2Te_3) being $n = 2 \times 10^{21}$ (6×10^{20}) cm^{-3}, $\mu = 1$ (5) $cm^2/V{\cdot}s$.

The switching dynamics of PCM devices were studied by applying voltage pulses to the devices and measuring their current response. Figure 1c shows a diagram of the measurement circuit. An initially crystalline GeTe (Sb_2Te_3) NW was first RESET by a voltage pulse 2.5 (2.3) V in height and 50 (50) ns in duration. The resistance increased by 3 (2−3) orders of magnitude in the GeTe (Sb_2Te_3) device after RESET. A SET pulse (1.1 (1.1) V, 100 (50) ns in GeTe (Sb_2Te_3)) was then applied. Figure 1d shows the voltage and current response of a representative GeTe NW device. The current increased from the noise level (<0.01 mA) to 0.26 mA in ~3 ns after the onset of the pulse voltage, limited only by the risetime of the pulse generator (a switching time less than 0.15 ns has been reported in chalcogenide glass).[1] Significantly, a comparison of the two-probe and four-probe resistance measurements shows that the resistance changes induced by the SET and RESET pulses originate from the NW itself and not from the contact resistance (which

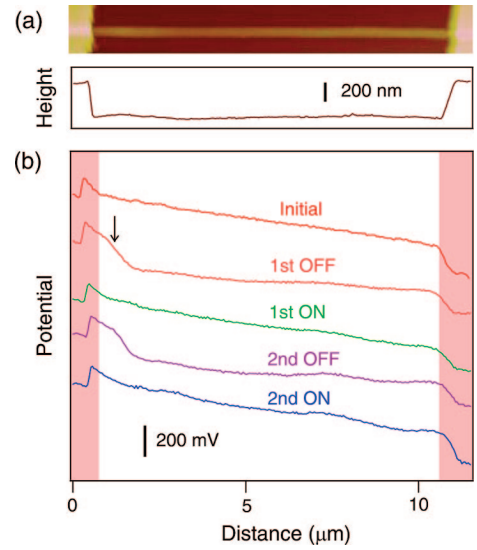

Figure 2. (a) AFM image and height profile along the NW length of a PCM device incorporating a single GeTe NW. (b) Surface potential profile along the NW length of the same device. On the potential curves, the region with a steep gradient, marked by an arrow, indicates the location of an amorphous domain. The shaded areas on the sides indicate the metal electrodes.

remained <100 Ω and unchanged throughout the switching sequence).

Measurements of the device resistance as a function of the SET pulse duration show that the SET process occurs through threshold switching followed by memory switching, similar to the mechanism in thin-film devices.[8,11] With a short pulse such as the one shown in Figure 1d (pulse width 100 ns), the device did not stabilize in the ON state and spontaneously returned to the OFF state; this observation indicates that while a short pulse can induce threshold switching, it is not long enough to cause memory switching. To estimate the minimal pulse width for memory switching, a series of pulses with increasing widths (50 ns to 1 μs) and a fixed pulse height (1.1 V) was applied, while the steady-state low-bias conductance (G_{AP}) of the NW was monitored after each pulse. Figure 1e shows G_{AP} as a function of pulse width: G_{AP} starts to increase once the pulse duration exceeds ~130 ns (70 ns) for GeTe (Sb_2Te_3) and reaches the stable crystalline-state conductance for pulses longer than 300 ns (200 ns). Measurements of multiple devices show that the time required for memory switching increases with the OFF state resistance (R_{OFF}) and has a range from 200 ns to 1 μs.

Kelvin probe microscopy (KPM)[23] enables the direct measurement of the surface potential profile of a NW device. Figure 2 shows representative atomic force microscope (AFM) and KPM images obtained for a 120 nm diameter GeTe NW device covered with a 40 nm thick layer of silicon dioxide. Topographically, the NW appears smooth throughout the SET and RESET switching. After RESET, a clear potential drop (0.2 V in height and 500 nm in length) is evident near the left electrode in the KPM scan, indicating the formation of an amorphous domain. In contrast, the ON state exhibits a smooth potential drop along the NW. From the measurements of more than 20 devices, we found that the insulating domains can appear anywhere along the NW,

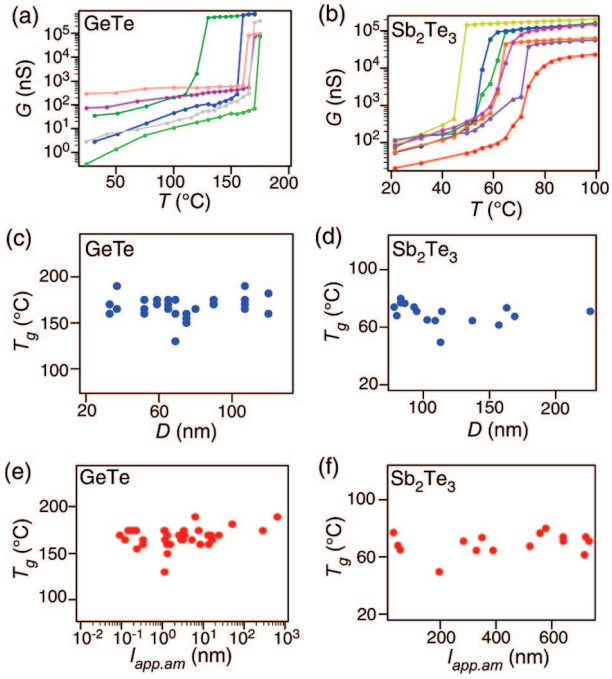

Figure 3. (a,b) Changes in the electrical conductance (G) upon the amorphous-to-crystalline phase change of GeTe and Sb_2Te_3 NWs as the temperature (T) is raised. (c−f) T_g of amorphous GeTe and Sb_2Te_3 NWs as a function of NW diameter (D) and $l_{app.am}$, respectively.

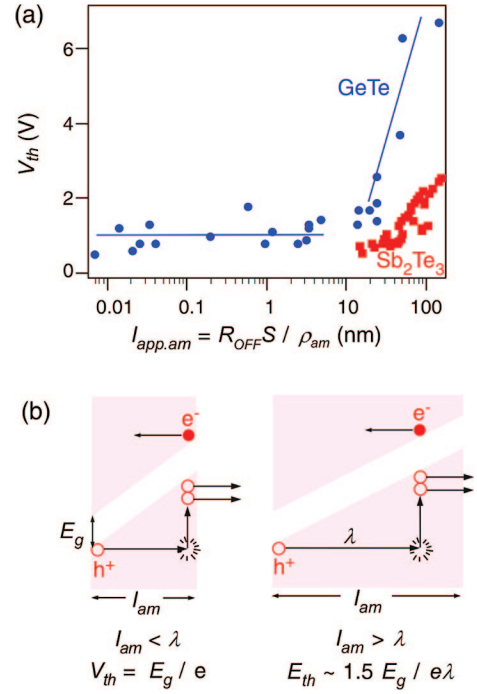

Figure 4. (a) $l_{app.am}$ dependence of V_{th} gathered from switching processes of multiple NW devices using voltage pulses with 100 ns duration. The lines are guides to the eye. (b) Schematic diagrams of the inelastic scattering processes that occur for $l_{am} < \lambda$ (left) and $l_{am} > \lambda$ (right).

not just near the contacts. Upon repeated ON-OFF cycling of a given device, however, an insulating domain always appears at the same location. These observations suggest that while the location at which the amorphous domain first appears is dictated by the initial defect distribution in a given NW, once an amorphization domain is formed, it serves as the "hot spot" where the subsequent melting process occurs.

The KPM image in Figure 2 clearly illustrates that the ON and OFF switching in our NW devices occurs via the formation of a small amorphous domain. It does not provide an accurate measure of the domain size (l_{am}), because of the finite scanning probe size and the long-range electrostatic interaction responsible for noncontact KPM imaging (see Supporting Information).[23] In fact, the amorphous domain size measured by KPM (typically ~500 nm) is a gross overestimation of the actual value, as demonstrated by the fact that the NW diameter that appears in the KPM scan (~800 nm) is much larger than the actual NW diameter (120 nm). A more reasonable measure of domain size can be obtained from the OFF-state resistance (R_{OFF}) by defining the apparent amorphous domain size as $l_{app.am} = R_{OFF}S/\rho_{am}$. Here S is the NW's cross-sectional area, and ρ_{am} is the amorphous thin-film resistivity (ρ_{am} (GeTe) ~ 10^4 Ω•cm and ρ_{am} (Sb_2Te_3) ~ 50 Ω•cm).[24,25] It should be clearly noted that $l_{app.am}$ is an underestimation of the true amorphous domain size (l_{am}), as can be seen in Figures 3 and 4 where the values of $l_{app.am}$ reach down to an unphysical 0.01 nm. This discrepancy arises because the melt-quenched amorphous domain may contain regions of partially crystalline phases,[26,27] and in thick nanowires multiple domains can coexist along the NW cross section. Nevertheless, we believe that $l_{app.am}$ provides a reasonable estimate of l_{am} above a few nanometers due to the large resistivity contrast in the amorphous and crystalline phases of GeTe and Sb_2Te_3 (ρ_{am}/ρ_{cryst} (GeTe) = 10^7 and ρ_{am}/ρ_{cryst} (Sb_2Te_3) = 10^4).[24,25]

Previous studies have shown that when the film thickness falls below ~35 nm, the glass transition temperature (T_g) of chalcogenide materials can increase because of reduced ion diffusion.[28] To examine whether such an effect is operative in our NW devices, T_g of amorphous GeTe (Sb_2Te_3) NWs with diameters ranging from 30 (78) to 120 nm (226 nm) was measured by monitoring the wires' conductance at small bias (<50 mV) as the temperature was slowly raised (<1 °C/min) under vacuum. Generally, the device conductance increased several orders of magnitude within a few degrees (Figure 3a,b), allowing a precise determination of T_g. As seen in Figure 3, NWs generally exhibit T_g values comparable to their thin-film counterparts (T_g = 145 °C for GeTe and 77 °C for Sb_2Te_3).[28,29] The T_g values do not exhibit clear correlations with either NW diameter or $l_{app.am}$, but they do show variations from device to device and also for different switching events in the same device. The microscopic reason for this fluctuation is not clear, but it might be related to variation in the exact domain/lattice configuration. The strain from the protecting oxide can be ruled out as a major contributor to the variation in T_g, since NWs not covered with silicon dioxide or nitride show similar behavior.

Unlike T_g, V_{th} shows a clear scaling behavior with $l_{app.am}$. In Figure 4a, the values of V_{th} measured with the 100 ns pulse are plotted against $l_{app.am}$. At large values of $l_{app.am}$, V_{th} of the NW devices increases linearly with $l_{app.am}$, indicating that E_{th} is 50 V/μm for GeTe and 20 V/μm for Sb_2Te_3. This

behavior clearly indicates that when $l_{app.am}$ is large, the threshold switching in our NW-based devices follows the same constant field scaling as seen in previous studies.[4,13]

As $l_{app.am}$ falls below ~10 nm in GeTe devices, V_{th} stops decreasing and reaches a minimum value (~0.8 V). In Sb_2Te_3 devices, the small values of $l_{app.am}$ were much harder to realize: even when the devices exhibited small R_{OFF}, the OFF state was unstable and spontaneously returned to the ON state over time. The stability difference of small amorphous domains in GeTe and Sb_2Te_3 most likely originates from the difference in T_g[28,29] and the weak bonding energy of Sb_2Te_3.[30] Nevertheless, Figure 4a shows that the $V_{th}-l_{app.am}$ curve for Sb_2Te_3 devices also starts to flatten when V_{th} approaches ~0.6 V. Overall, the data presented in Figure 4a demonstrates that the scaling law governing threshold switching changes from constant field scaling at large amorphous domain sizes to constant voltage scaling at smaller sizes.

The crossover of the $V_{th}-l_{app.am}$ scaling can be understood using the impact ionization model, which has been invoked to explain threshold switching,[11] and it provides strong experimental evidence for the validity of the model. During threshold switching, the charge carriers moving through the amorphous phase are accelerated by the applied electric field and collide inelastically with phonons. If the field is high enough and the carriers acquire enough kinetic energy, collisions generate electron−hole pairs via inelastic scattering, which leads to carrier multiplication and thus an avalanche process. When l_{am} is smaller than the carrier mean free-path, λ, (Figure 4b) the voltage drop across the domain must exceed the band gap of the amorphous phase (E_g/e where e is electron charge) for carrier multiplication to begin. Values of minimum V_{th} observed at small values of $l_{app.am}$ in Figure 4a are indeed close to E_g/e of amorphous GeTe and Sb_2Te_3 (0.8 V and 0.5−0.8 V, respectively).[25,31] These values can therefore be understood as the direct consequence of a simple energetic requirement for carrier multiplication.

When l_{am} is larger than λ, the important parameter for carrier multiplication is the kinetic energy gained by the carrier over λ (Figure 4b). According to a theoretical model[32] that integrates conservation of energy and momentum, the critical field required for carrier multiplication is given by $E_{th} = 1.5\ E_g/e\lambda$. The values of E_{th} determined in our experiment (which agree well with previous results)[4] then translate to λ values for amorphous GeTe and Sb_2Te_3 of ~20 and ~50 nm, respectively. It should be clearly noted that because $l_{app.am}$ is an underestimation of the true domain length, these λ values are only approximate.

The existence of a minimum V_{th} in the SET switching has an important implication for the scalability of PCM cells to nanoscale dimensions. Were V_{th} to follow the constant field scaling observed at large l_{am} down to the nanometer scale, the OFF state would become electrothermally unstable and could be switched on spontaneously by small voltage fluctuations. The minimum V_{th} at small $l_{app.am}$ observed in our experiment indicates that the size of PCM bits can be miniaturized to a true nanometer scale without unintentional data loss.

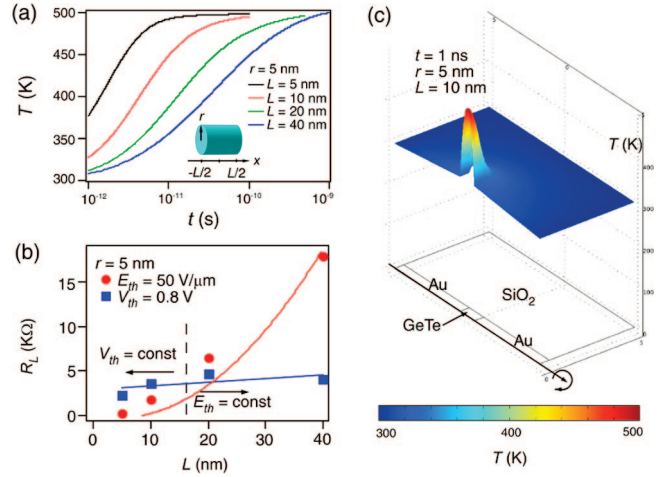

Figure 5. (a) Temperature (T) evolution during SET processes at the center of NW-PCM cells with different device lengths (L). The current (I) was turned on at $t = 0$, and the magnitude of the current was chosen to heat the memory cell to ~500 K (I = 0.278, 0.163, 0.110, 0.087 mA at L = 5, 10, 20, 40 nm, respectively). (Inset) Schematic of PCM cell geometry. (b) R_L as a function of L for the cases of both constant V_{th} and E_{th} scaling. The data were fitted by the analytical form of R_L as discussed in Supporting Information. The vertical dashed line separates the V_{th}- and E_{th}-constant regimes. (c) Representative temperature profile at $t = 1$ ns after the current was turned on ($L = 2r = 10$ nm). The cylindrical device can be visualized by rotating the cross-section of the device around the axis in the bottom part of the figure.

It should also be noted that the minimum V_{th} found in this study impacts the circuit design of nanoscale PCM cells. During a SET process of a PCM cell, a serial load resistor (R_L) is usually included in the circuit to limit the current and to achieve the suitable annealing temperature. Simple analytical considerations as well as numerical simulations[33] suggest that the crossover of the $V_{th}-l_{app.am}$ scaling and the existence of a minimum V_{th} reported here alters the optimal choice of R_L values as a function of PCM cell size (see Supporting Information). Specifically, simulations of the planar devices studied here indicate that, when the threshold voltage scaling relation changes from constant field to constant voltage, the optimal R_L values for 10 nm diameter GeTe PCM cells increase from 1.8 to 3.6 kΩ for 10 nm thick cells and from 0.3 to 2.2 kΩ for 5 nm thick cells (Figure 5). Although the details of the device architecture will change these quantitative predictions, they nevertheless suggest that the inclusion of the proper V_{th} scaling is important in the design of PCM cells and their supporting electronics.

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Supporting Information Available: The details of fabrication, electrical characterization, KPM measurements, and the load resistance scaling simulation of NW-PCM devices. This material is available free of charge via the Internet at http://pubs.acs.org.

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